Inverse Lithography Technology at Low k1: Placement and Accuracy of Assist Features

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ABSTRACT

An implementation of inverse lithography technology is studied with special attention to illustrating and analyzing the placement, accuracy, and efficacy of subresolution assist elements. One-dimensional placement through pitch is characterized, and 2D capability is demonstrated for repeated patterns. Differences between the methods of mask preparation afforded by this system as compared to current practices are described.

Keywords: Inverse Lithography Technology, ILT, OPC, RET, SRAF

1. INTRODUCTION

Deep sub-wavelength imaging is a continuing challenge for the semiconductor industry. Several resolution enhancement techniques (RETs) are currently employed broadly to meet this challenge. Off-axis illumination, careful mask patterning, and attenuated phase shift mask technology are routinely applied RETs for 65nm and newer processes. Subresolution assist feature (SRAF) placement, a key component of mask patterning, is the subject of this study.

SRAFs are commonly used in the industry, even though they entail costs on the part of the semiconductor manufacturer. The first cost is in mask writing. Consider a contact hole mask: adding one rectangular SRAF per rectangular contact feature doubles the mask data volume and may significantly increase write time (for vector-based e-beam mask writers); typically more than one SRAF per contact is needed to optimize image fidelity.

Secondly, there is a less tangible but still important productivity cost. SRAF placement in current practice is not fully automated (though important attempts have been made [1-3]). A typical sequence in lithographic process development is:

a) select the illumination
b) run a series of simulations to characterize the optimal shape and placement of SRAFs for characteristic design patterns
c) create a script which places the SRAFs according to a recipe determined from step b
d) "freeze" the placed SRAFs and compute the rest of the mask.

Steps b and c are time-intensive, and step d is essentially open-loop, that is, the success in the final mask preparation is not guaranteed, since there may well be geometric configurations in the immense selection of full-chip locations that were not studied in step b and scripted in step c. Particularly, the target features may not print to the specified quality, and side-lobe printing may occur at locations corresponding to placed SRAFs. This may lead to a step that creates an iterative loop:

e) run lithographic verification on the output of step d, and repeat the process beginning at steps a, b or c as needed.

This paper describes the use of one implementation of inverse lithography technology (ILT) [4] in preparing SRAFs for semiconductor masks. The properties, accuracy, efficacy and costs of this alternative technology are addressed using multiple lithographic examples. Except where mentioned explicitly, all simulation results are prepared using the optical modeling capabilities of Luminescent ILT. Its modeling has been checked against three industry standard optical modeling software packages by Luminescent, and has been independently audited and/or checked by lithographers at various semiconductor companies.

2. PLACEMENT ACROSS PITCH

To illustrate the adaptive properties of this implementation of inverse lithography in one dimension, a series of regular one dimensional gratings with varying pitch is used with realistic design and lithographic parameters. Figure 1 shows a selection of 70 nm darkfield gratings, varying in pitch from 210nm to 800nm.

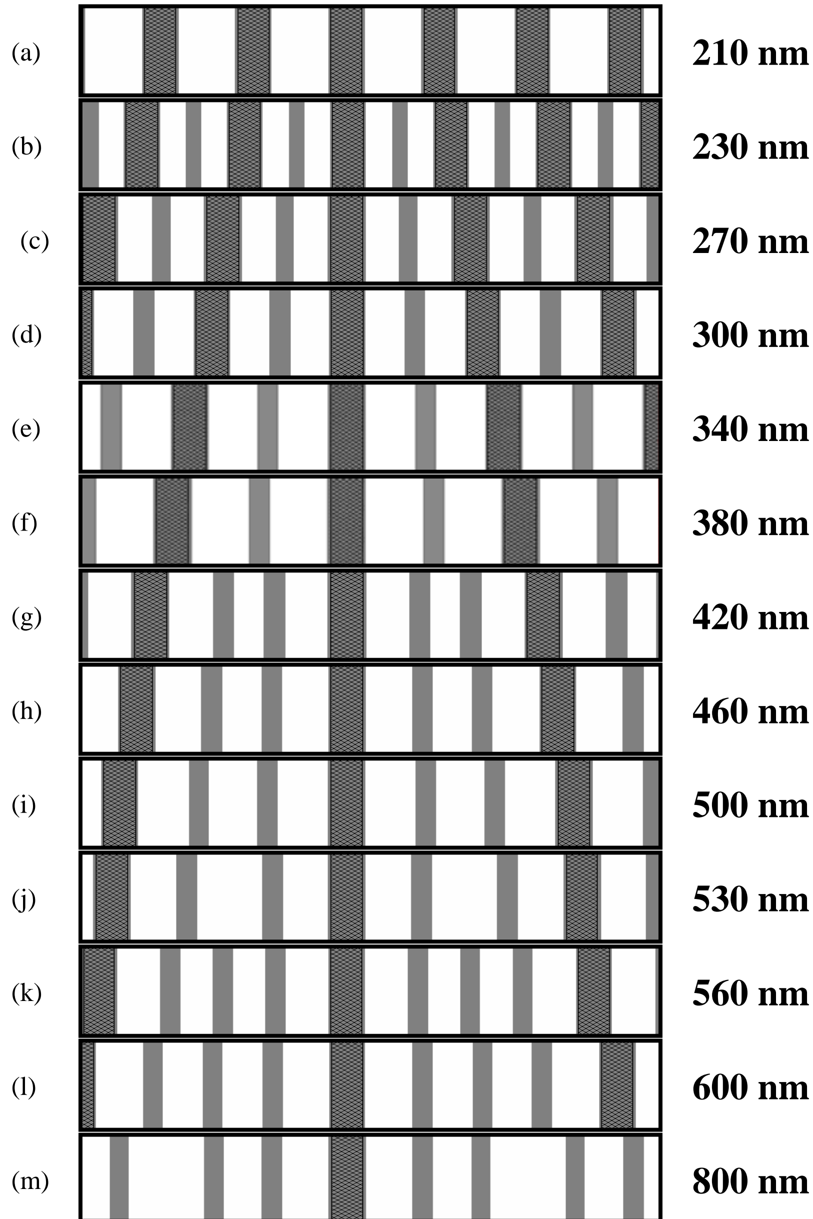


Fig.1. Simultaneous mask creation and SRAF placement using ILT for regular gratings. As the pitch of the 70nm grating elements is varied from 210nm to 800nm, (a)-(m), the number, position, and width of inter-feature SRAFs is adjusted automatically.

The optical conditions used are: 193nm wavelength, annular illumination with inner sigma of 0.6, outer sigma of 0.85, and numerical aperture of 0.87. A 6% attenuated phase shift mask and a constant threshold

model are used in the simulation, and the inversion goal is set so as to a) minimize edge placement error (EPE) and b) maximize process window, including maximizing image log slope (ILS) at three dose-focus conditions. Two families of production constraints are used: imaging reliability and mask manufacturability. For imaging reliability, side-lobe printing is to be avoided over a +- 20% (of nominal) dosage range; for mask manufacturability, mask widths lower than 25 nm and mask spaces lower than 25 nm are not allowed.

Under these conditions and constraints, the simultaneous creation of mask elements overlying the design features and assist figures distinct from design features has four notable properties within the scope of this study:

1. The assist features are added as the pitch increases. Compare, for example, Figs. 1a and 1b, 1f and 1g, and 1j and 1k.
2. The spacing between assist features grows for increasing pitch but fixed numbers of assist features (Fig 1b-1f, for example).
3. The assist feature size changes for increasing pitch but fixed numbers of assist features, e.g., in Figs. 1b-1c.
4. The “main” mask features, that is, the mask elements overlying the original design features also change in width for increasing pitch but fixed numbers of assist features (compare Figs. 1a and 1b, for example).

The first two properties are well known in current sub-resolution semiconductor lithography, and can be replicated with a variety of automatic methods. The third and fourth properties are more subtle and observable only after a formal lithographic design of experiments (DOE). In current practice, this involves either manual or deliberate, exhaustive place-and-image experimentation. Designers of regular, repetitive integrated circuits such as memories have long used such DOEs to replicate these properties on small structures such as a single memory cell. Automation of these latter properties has been elusive; memory mask design continues to rely on exhaustive crafting for optical optimization, and logic masks are not presently optimized on an area-by-area basis – though advanced logic mask are optically enhanced with a global, nonadaptive recipes. An automated adaptive approach that displays all four properties observed from Figure 1 can therefore advance mask design productivity.

To verify the efficacy of SRAF placement, the 500nm pitch case (Figure 1i) is chosen. As with all of these cases, the simulation was run with a three image model – that is, with the directive to minimize EPE at 3 locations in the focus-exposure space [4]. Specifically, nominal dose and positive 90nm defocus (anchor point A), nominal focus at 95% of nominal dose (anchor point B) and nominal focus at 105% of nominal dose (anchor point C) were chosen. The system reports EPE at each of these anchor points as well as the nominal focus-exposure point. As shown in Table 1, EPE improves at the nominal conditions and all anchor points for this 70nm feature, except the positive defocus point A. For point A, the difference is ~ 0.5 nm, which is negligible. For the others, the differences are in the 2-3.5nm range, which are significant.

Anchor point	Dosage (percentage from nominal)	Focus (nm from nominal)	EPE (nm) without SRAFs	EPE (nm) with SRAFs
Nominal	100%	0	4.28	1.89
A	100%	+90	0.06	0.61
B	95%	0	8.18	4.82
C	105%	0	2.99	1.04

Table 1. Efficacy of the SRAF placement of Figure 1i (500nm pitch grating).

As a second method of verification, forward images were computed during the simulation for Figure 1i for dosages 80% and 120% of nominal, at nominal focus, and for focus conditions of -150nm and +150nm from nominal, at nominal dose. No sidelobes were observed in any of the four images.

Before leaving this example, a note is required regarding an important trade-off that must be made when using SRAFs. We specified at the beginning of this section that both sidelobe avoidance over a given exposure range and a SRAF minimum width are enforced in these simulations. These two goals are not always compatible. For example, setting the SRAF minimum width to 80nm would probably produce sidelobe printing at nominal dose. The system will “do the best it can” to adjust the SRAF distance, the main feature mask element size, etc., when faced with a challenging minimum SRAF dimension. However, for widths larger than physically appropriate, it will remove the SRAF from the mask pattern and/or warn that image fidelity does not meet specifications.

3. OPTICAL BEHAVIOR

The example illustrated in Figure 2 tests two aspects of this inverse lithography method: robustness to optical orientation and process window improvement. A cruciform pattern (2a) with 80 nm vertical and horizontal elements is imaged with a dipole illuminator (2b). The wavelength is 193 nm, and the numerical

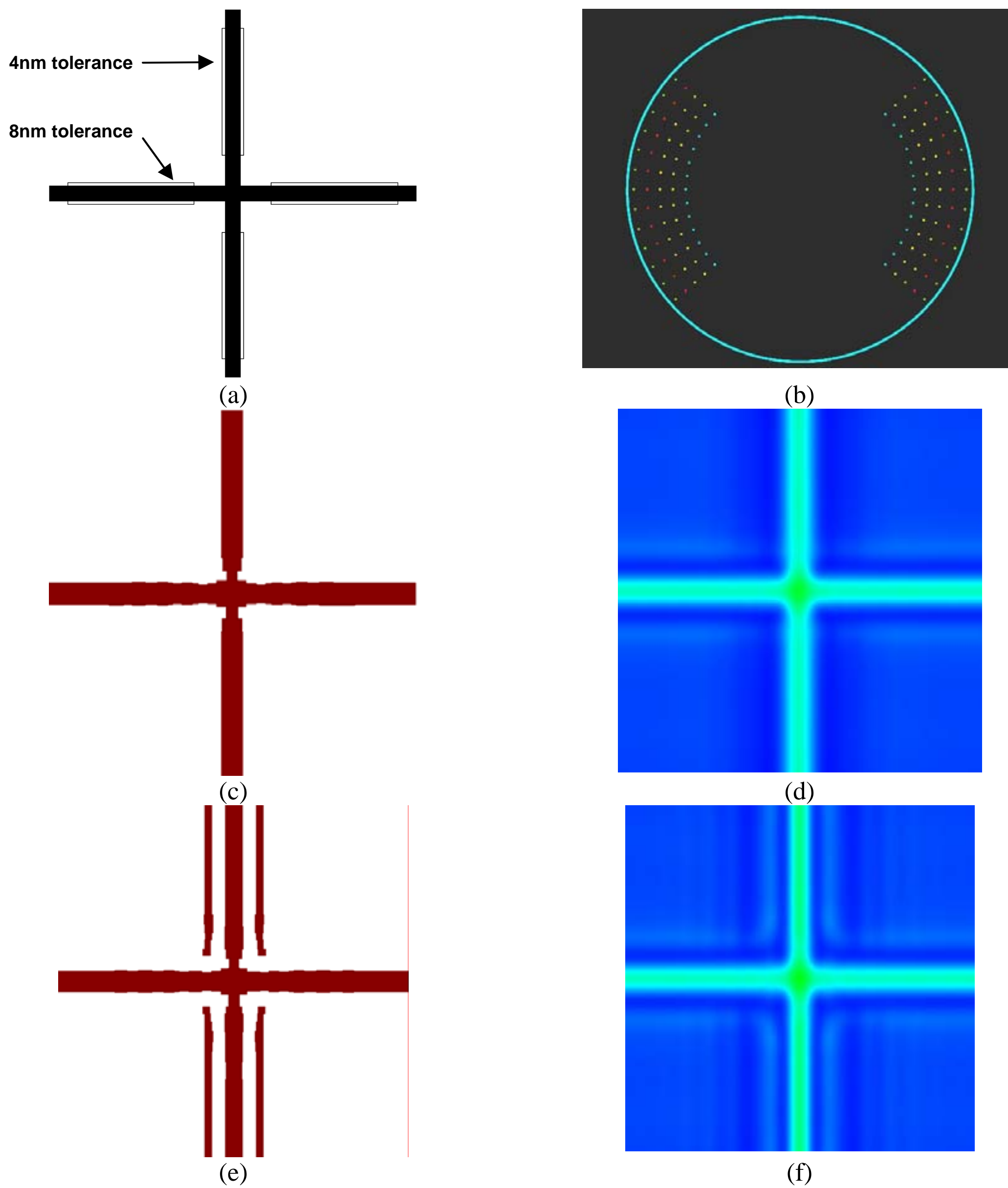


Fig.2. Auto-SRAF creation with nonstandard illumination. a) 80nm target (solid) with overlaid critical regions (outlined). b) Light source c) ILT mask with auto-SRAFs disabled. d) The intensity image from c). e) Computed mask with auto-SRAF enabled. Only vertical SRAFs are added, due to the dipole orientation. f) The intensity image from e).

aperture is 0.85 with outer sigma of 0.95 and inner sigma of 0.65. A constant threshold vector model is used with a representative resist film stack; a darkfield 6% attenuated phase shift mask is selected as the target mask technology for inversion.

The on-wafer target is shown in Fig. 2a as a filled cruciform polygon. For reporting process window, a worst-case EPE metric is used for all of the results of this experiment with sub-nanometer resolution in the four outlined (non-filled) polygons (critical regions) of Fig. 2a. Specifically, for the reported results of this experiment, the vertical critical regions are given a worst-case EPE tolerance of 4nm and the horizontal critical regions are given a worst-case EPE tolerance of 8nm. This factor of two difference in process window tolerance is consistent with expectations that the dipole illumination of Figure 2b will better resolve vertically oriented features.

Only "primary" assist features are allowed in these simulations. That is, the center of each optical assist element on the mask is constrained to lie within a distance from the edge of a design element equal to half of an effective optical wavelength λ/NA. The mask is computed with mask manufacturability constraints as follows: mask widths lower than 40 nm and mask spaces lower than 35nm are not allowed. Lastly, the inversion goal is specified as follows: the worst case EPE should meet 4nm in the vertical critical region and 8nm in the horizontal critical region for the three focus-exposure points of nominal focus and exposure, nominal exposure with focus +40nm off of nominal focus, and nominal exposure with focus -40nm off of nominal focus.

As an experimental control, the target design of Figure 2a is imaged, without ILT or any other sort of mask creation. No process window is obtained in simulating with the aforesaid conditions.

A mask with only "main" features, that is, features that overlie the wafer target, results in the mask of Figure 2c after ILT. The corresponding intensity distribution is shown in Figure 2d. The mask of Figure 2c produces an absolute exposure latitude (EL) of 4.3% of nominal exposure and no focus latitude for the specified 5% EL threshold. Allowing a primary assist feature as defined above, the mask of Figure 2e is computed, with a corresponding intensity distribution shown in Figure 2f. This mask produces an exposure latitude of 11.5% of nominal exposure and a focus latitude of 183 nm at 5% EL.

Two observations are notable from this exercise. First, the inversion algorithm used creates assist features that are predominantly vertical given a light source that strongly favors assist features of this orientation. There is some curvature of the largely vertical assist feature near the horizontal design element that is not addressed in this study but may warrant further investigation; there are no horizontal assist elements parallel to the horizontal design element. Second, this implementation of ILT succeeds in simultaneously creating a main mask feature and an optical assist feature that strongly improves a strict process window requirement. While not explicitly demonstrated in this example, we suspect that all four properties of this ILT implementation noted from the varying-pitch examples illustrated in Figure 1 contribute to the improvement of on-silicon process window demonstrated in the example illustrated in Figure 2.

5. PLACEMENT ACCURACY

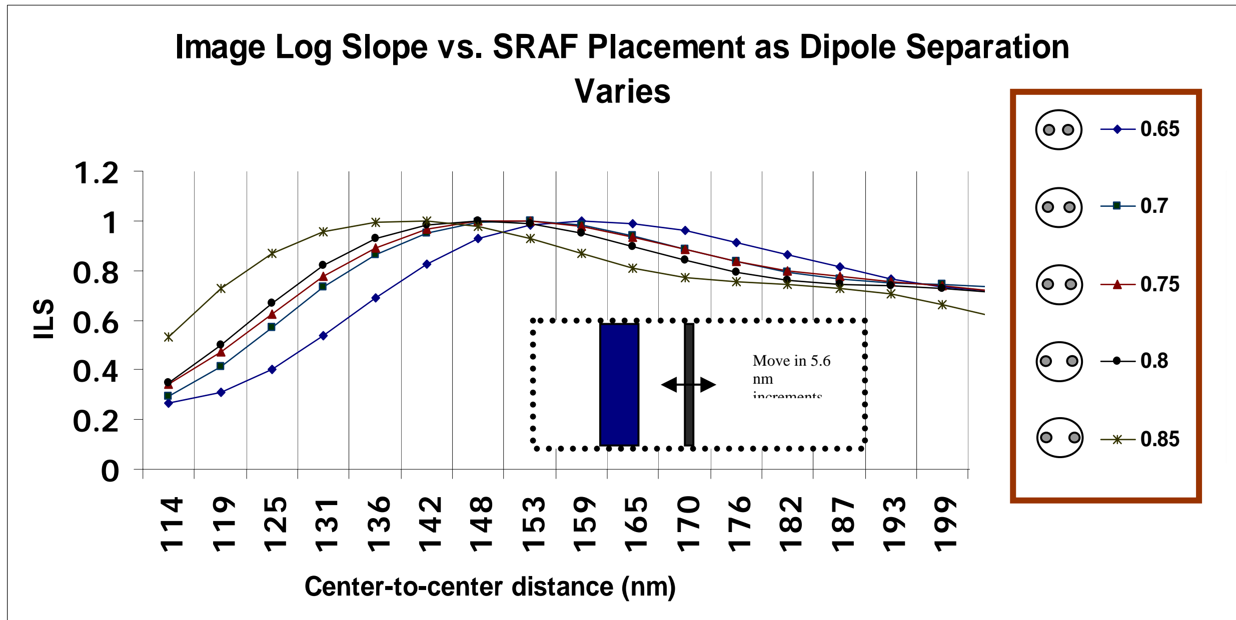
Regardless of whether an adaptive mask creation method such as ILT has the useful properties discussed in the first experiment of this study, and has the proper optical orientation behavior shown in the second experiment (previous two sections), it must be accurate and optically efficacious to be of relevance to lithographers. In this section, the assist feature placement of the implementation of ILT used in this study is compared with placements determined with a commonly used commercial simulator. The presumption is that the commercial simulator has been extensively benchmarked and proven accurate in several independent studies by lithographers at semiconductor manufacturers and therefore is a “golden standard” of accuracy.

Figure 3 illustrates the experiment. To establish a baseline result (Figure 3a), the commercial simulator from Panoramic Technology [see, for example, reference 5] is used to image a vertical 90nm feature with 193nm wavelength dipole illumination and a numerical aperture of 0.85. A total of 80 simulations are conducted as follows. Five different dipole configurations (dipole elements centered at radii of 0.65, 0.70, 0.75, 0.80, and 0.85 within the aperture) are chosen, and for each illuminant configuration, a single 40nm rectangular assist bar is placed in one of 16 distances as measured from the center of the SRAF to the center of the 90nm feature. The distances range from 114nm to 199nm in 5.6nm increments. Image log slope (ILS) is measured in each simulation, and plotted against distance to yield the 5 curves of Figure 3a. The distance that yields the peak image log slope is noted and plotted in Figure 3b.

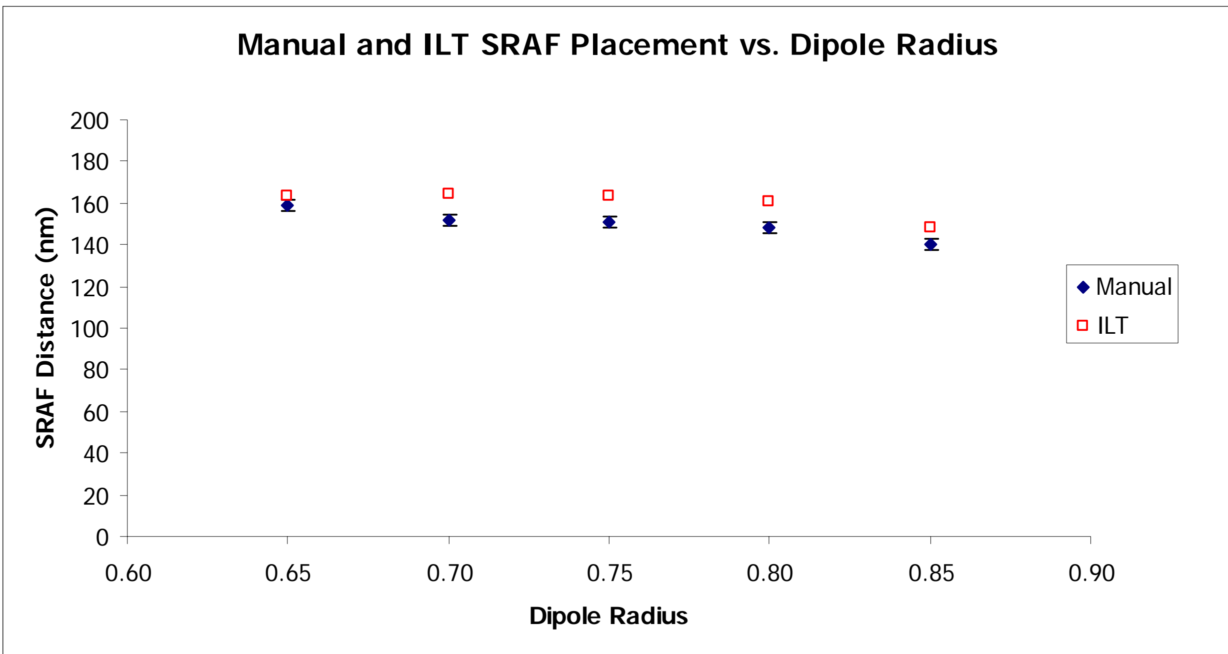
Secondly, five runs of the implementation of inverse lithography technology under study are carried out, one for each of the 5 dipole configurations. For each ILT run, the mask geometry overlying the 90nm feature and subresolution mask elements are computed simultaneously; the simulation is constrained to produce a single assist feature on either side of the 90nm feature, with mask constraints as detailed in the previous sections of this paper. The center-to-center distance from the drawn 90nm feature and the assist feature is measured and also plotted in Figure 3b.

The implementation of inverse lithography technology under study consistently separates the assist feature more than the optimal manual placement (range 5nm-13nm, average 10nm). While the differences between the two sets of results is not large, they are understandable. First, the implementation of ILT under study optimizes more than ILS; EPE is strongly weighed in this implementation, for example [4]. Second, and probably more importantly, the ILT system used does not “freeze” the size of the mask assist element and the size of the mask element overlying the main 90nm feature while determining optimal assist feature placement. Rather, it adjusts both to optimize the total outcome. In this experiment, the adaptive ILT system under study simultaneously varies the assist feature distance from the main feature, the assist feature size, and the main mask feature size (properties two, three, and four discussed in section 2).

To summarize this experiment, it can be said that the ILT system under investigation places assist elements with a degree of efficacy close to that of a manual “freeze and place” method. The placement distances are close to those found in the manual method, but not identical.



(a)



(b)

Fig.3. Verification of ILT SRAF placement efficacy. Using a commercial lithographic simulator, 16 SRAFs were manually placed in proximity to a 90nm vertical feature in increments of 5.6 nm distance from the feature, for 5 dipole configurations. Image log slope for each placement is shown in (a). ILT placement was then characterized for each dipole, and plotted with the optimum manual placement in (b). Error bars for the manual points are +- 2.8nm.

5. TWO DIMENSIONAL EXAMPLES

In this last section, two-dimensional patterns are chosen for mask creation according to their relevance to the semiconductor manufacturing industry. This industry routinely processes countless image patterns from various locations in the thousands of design layers manufactured annually. The patterns can be broadly lumped into to two categories: interconnect patterns and hole patterns. In this section, regular, repeated 2D structures are simulated. A study of structures of less regular, more random nature is in preparation.

Figure 4a shows an SRAM bit cell pattern of feature size 80nm, first described with reference to ILT in [6]. The simulation conditions are as follows: 193nm wavelength, a numerical aperture of 0.84, annular illumination with inner sigma of 0.64 and outer sigma of 0.93, a vector model with a representative film stack, a darkfield 6% attenuated phase shift mask and periodic boundary conditions. The mask manufacturability constraints are: main feature minimum spacing and width of 40nm, and SRAF minimum spacing and width of 50nm. Primary SRAFs are allowed.

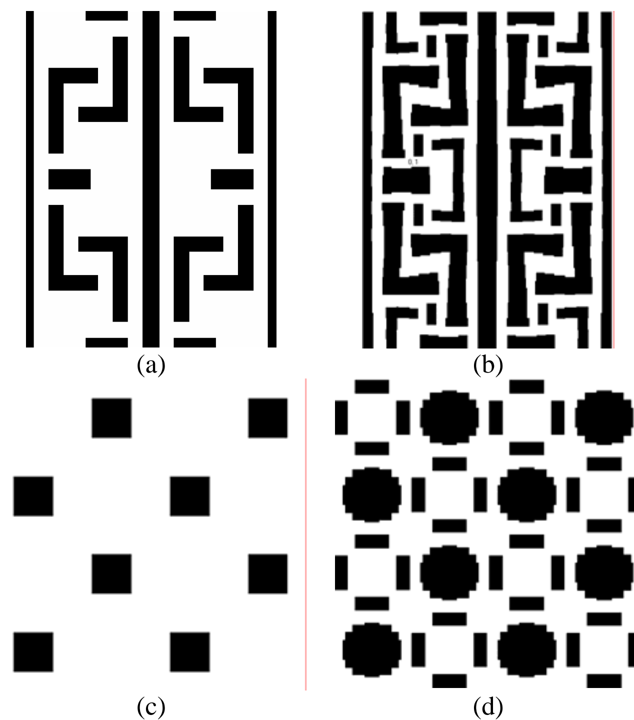


Fig.4. Auto-SRAF placement for repeated two dimensional design patterns. (a) 65nm SRAM bit cell interconnect layer design and (b) corresponding mask. (c) 45nm contact hole layer design clip and (d) corresponding mask.

The result shown in Figure 4b shows: a) long, straight vertical elements of the design are modulated slightly according to local (~100nm radius) conditions; b) horizontally oriented design rectangles are transformed into dog-bone-shaped structures on the mask, with narrow hammerheads in dense regions and broader hammerheads in semi-isolated regions; c) “L” shapes taper inwards from the outer extent of the “L” to a minimum width at the corner of the “L”; assist elements are placed to fill empty regions in the design; both simple rectangular SRAFs and more complex, width-modulated “C” shaped SRAF structures are created.

Figure 4c shows a regular, skewed contact hole array of feature size 128nm. The simulation conditions are as follows: 193nm wavelength, a numerical aperture of 0.85, annular illumination with inner sigma of 0.66 and outer sigma of 0.96, a vector model with a representative film stack, a darkfield 6% attenuated phase shift mask and periodic boundary conditions. In computing this mask solution, the system was restricted from placing SRAFs along the diagonals of the main features in this study. Mask width/space constraints were not applied in this example, and only primary SRAFs were allowed. The computed mask in Figure 4d shows contact main feature mask elements that are 3 fragments per side, so as to fracture at 9 or fewer shots, and simple rectangular subresolution assist elements placed at cardinal positions (north, east, south, west) with respect to the contact feature.

CONCLUSIONS

In a simulation study, four sets of examples were studied to illustrate and analyze an implementation of inverse lithography technology, especially with regard to its ability to place subresolution assist features of significance to lithographers. 1) A set of gratings varying in pitch pointed to four properties of the implementation, two of which may have significance in increasing the productivity of semiconductor mask preparation. One grating was selected; a mask with automatically placed SRAFs computed to image the grating was shown to produce improved on-wafer pattern fidelity across a set of focus and exposure points as compared to a mask for the same grating without SRAFs. 2) A mask with automatically placed SRAFs computed for a cruciform pattern illuminated with a dipole revealed that the SRAF placement is correctly oriented with respect to optical physics. A process window analysis of this mask pattern showed improved exposure latitude and depth of focus as compared to simple imaging of the target pattern and imaging of a mask pattern computed without SRAFs. 3) Automatically placed SRAFs to assist in imaging of a single line were compared to a series of manually placed SRAFs by means of measuring the resultant on-wafer image log slope, as determined with an independent commercial lithography simulation package. The manual and automated approaches were largely in agreement, with minor differences attributable to the whole-image optimization behavior of the ILT system under study. 4) Two dimensional patterns – one of a semiconductor interconnect layer and the other of a semiconductor contact layer – were chosen and masks computed for them given realistic lithographic conditions. A preliminary description of the 2D behavior of the system under study was provided using these example patterns. These studies demonstrate the ability of an adaptive approach such as ILT to efficaciously locate SRAFs in a diverse layout environment.

ACKNOWLEDGMENTS

The authors wish to express their gratitude to Artur Balasinski of Cypress Semiconductor for providing the SRAM bitcell pattern.

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